

FIN-TYPE DECOUPLING CAPACITORS

Abstract of the Disclosure

Device designs and methods are described for incorporating capacitors commonly used in planar CMOS technology into a FinFET based technology. A capacitor includes at least one single-crystal Fin structure having a top surface and a first side surface opposite a second side surface. Adjacent the top surface of the at least one Fin structure is at least one insulator structure. Adjacent the at least one insulator structure and over a portion of the at least one Fin structure is at least one conductor structure. Decoupling capacitors may be formed at the circuit device level using simple design changes within the same integration method, thereby allowing any number, combination, and/or type of decoupling capacitors to be fabricated easily along with other devices on the same substrate to provide effective decoupling capacitance in an area-efficient manner with superior high-frequency response.

Figures

Figure 1: A line graph showing the relationship between the number of figures and the number of pages. The x-axis represents the number of figures (0 to 10) and the y-axis represents the number of pages (0 to 10). The data points are as follows:

Number of Figures	Number of Pages
0	0
1	1
2	2
3	3
4	4
5	5
6	6
7	7
8	8
9	9
10	10